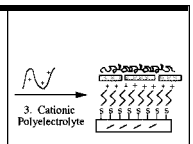
Self-assembly of single electron transistors and related devices



CHEMICAL SOCIETY REVIEWS

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For the past 40 years, since the invention of the integrated circuit, the number of transistors on a computer chip has doubled roughly every 18 months. As the limits of photolithography are rapidly approached, however, it is becoming clear that continued increases in circuit density will require fairly dramatic changes in the way transistors are designed and operated. This review summarizes current strategies for fabricating transistors which operate based on the flow of single electrons through nanometre-sized metal and semiconductor particles; *i.e.* single electron transistors (SETs). Because the room temperature operation of SETs requires nanoparticles < 10 nm in diameter, we focus mainly on devices which have the potential for being assembled from the solution phase (non-lithographic systems). Several applications of SETs are discussed in addition to the major hurdles which must be overcome for their implementation in electronic device technology.

1 Introduction

1.1 History and impact of the transistor

The fabrication of the first transistor by Shockley, Brattain and Bardeen nearly 50 years ago is arguably the most important technological development of the 20th century.[1] Indeed, it is difficult to think of an area of our lives on which the transistor has not had a significant impact. Transistors are major components in such comforts as compact disc players, high-performance automobiles, portable telephones and televisions and countless electronic devices. Perhaps more important to basic human health, transistors are found in portable sensors for rapid medical and environmental screening, may soon provide more freedom to diabetics *via* electronic wristwatch insulin-delivery systems and one day may aid in returning sight in certain cases of blindness through 'vision chips' implanted in the back of the eye.[2] Of course, the greatest triumph of the transistor is the personal computer, which now possesses more memory in the space of a small briefcase than computers which once filled large rooms.

The above examples were made possible because the transistor has shrunk incredibly in dimensions over the past 40 years. Fig. 1 shows a timeline of the transistor minimum feature size *vs.* year. The size of the transistor has decreased by a factor of 2 every 18 months, a trend first pointed out by Gordon Moore in the 1960s (Moore's Law) and one that continues today.[3] Today, electronic devices employed in state-of-the-art integrated circuitry have dimensions of the order of 0.35 μm (350 nm). Thus, well over 1 million transistors can be integrated in the space taken up by the first transistor.

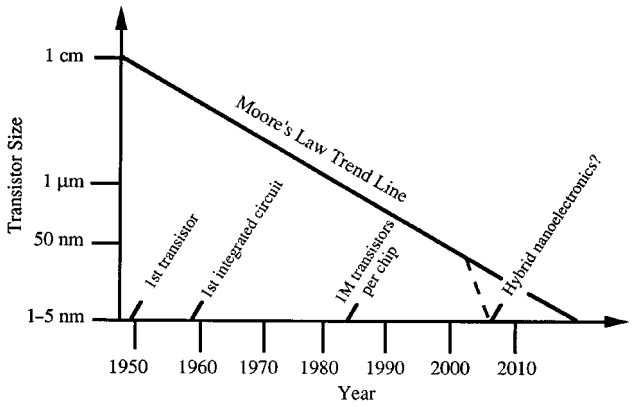

Fig. 1 "Moore's Law" plot of transistor size *vs.* year. The trend line illustrates the fact that the transistor size has decreased by a factor of 2 every 18 months since 1950.

This review addresses the question of how current trends may be continued in transistor miniaturization, ideally down to the molecular level (tens of nanometres or less). It is tempting to

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suggest that, as the resolution of surface patterning techniques such as electron beam lithography improves, conventional transistors could simply be made even smaller. Unfortunately, the electronic properties of solids and solid–solid interfaces are inherently different on the nanometre level. Thus, it is evident that if electronic integrated circuitry is to reach its ultimate potential (molecular-scale computing), radical changes in the way transistors are fabricated and operated will be necessary. But what will these changes entail? What materials will futuristic transistors be made from? How will they be assembled? How will they operate? The answers to these questions promise a revolution in the electronics industry. Consider that if the transistor could be scaled down to 5 nm in size, over 10 000 of these 'nanotransistors' would fit in the same area as one of today's transistors.

Many schemes for building nanometre-scale computer components have been proposed.[4] These include logic based on single molecules, molecular shuttles, resonant tunnelling diodes and atomic relays. Of all the designs proposed for use in futuristic integrated circuitry, the one receiving the most attention lately is perhaps the single electron transistor (SET).[5] (Coincidentally, this year marks the 100th anniversary of the discovery of the electron). The SET is similar in principle to the conventional field effect transistor (*vide infra*). Logic operations in the SET are based, however, on the tunnelling of single electrons through nanometre-sized metal or semiconductor quantum dots. In the discussions which follow, we describe the operating principles of the SET and related single electron devices. Several possible applications are highlighted, some of which have already been reduced in practice. The major obstacles to implementing single electron devices in computer technology are discussed in addition to some strategies which are being pursued to overcome these problems. While lithographic techniques are mentioned briefly throughout the review, because of size and cost constraints imposed on SETs, we focus mainly on devices which have the potential for assembling themselves, from solution, *via* chemical interactions. Our objectives are to present a chemist's view of the basics physics behind the SET (Section 2.1) and to summarize current efforts toward the chemical synthesis of SETs (Sections 3 and 4). Because space does not permit a general review of self-assembling systems, we have respectfully omitted many important works in this area, including those of Whitesides,[2,4] Stoddart,[4] Petty, Ferguson and others[4]. However, many of these papers are referenced within the literature cited at the conclusion of this manuscript.

1.2 The metal oxide semiconductor field effect transistor (MOSFET)

Before describing the SET, it will prove useful to briefly review the design and operating principles of conventional MOSFET transistors. The MOSFET is the most common type of transistor found in modern digital circuitry. A schematic diagram of an 'NMOSFET' is shown in Fig. 2(*a*).[6] The NMOSFET consists of highly conductive n-type Si source and drain regions separated by an insulating p-type Si channel and body. The letters n and p refer to atomic impurities or 'dopants' which add excess free negative or positive charges, respectively (the N in NMOSFET signifies n-type). Typical dopants for Si are boron or arsenic. Source and drain are terms which describe where current flows from and to, respectively. A metal electrode, commonly known as a gate, separated by a thin oxide layer is attached to the Si channel. In the absence of an applied voltage bias between the gate and body in an NMOSFET, current cannot flow between the source and drain because the p-type channel is insulating (the 'off' state). Upon application of a positive potential to the gate, electrons migrate into the channel essentially creating an n-doped conductive pathway between the source and drain (the 'on' state). Since the NMOSFET is off in the absence of an applied bias, it is sometimes called a 'normally off' transistor. This behaviour may be contrasted with the n-channel MOSFET in which a thin n-type channel has been inserted under the oxide layer between the source and drain regions [Fig. 2(*b*)]. In the absence of an applied gate bias a conductive path exists between the source and drain. When a negative potential is applied to the gate electrons are forced out of the channel. This renders the channel p-type (insulating) and eliminates the current path between the source and drain. Since the n-channel MOSFET is on in the absence of an applied bias, it is called a 'normally on' transistor. Similar devices are made with p-type channels (PMOSFETS). When these two-state (on/off, 1/0) transistors are integrated together on one chip, they are called complimentary MOSFETs (CMOSFETS). Various combinations of CMOS transistors provide the NOT, OR, AND, *etc*. logic functions upon which computer operations are based.

A second important function of the MOSFET is signal amplification. Amplification in a transistor is due to the acceleration of electrons as they move through the strong

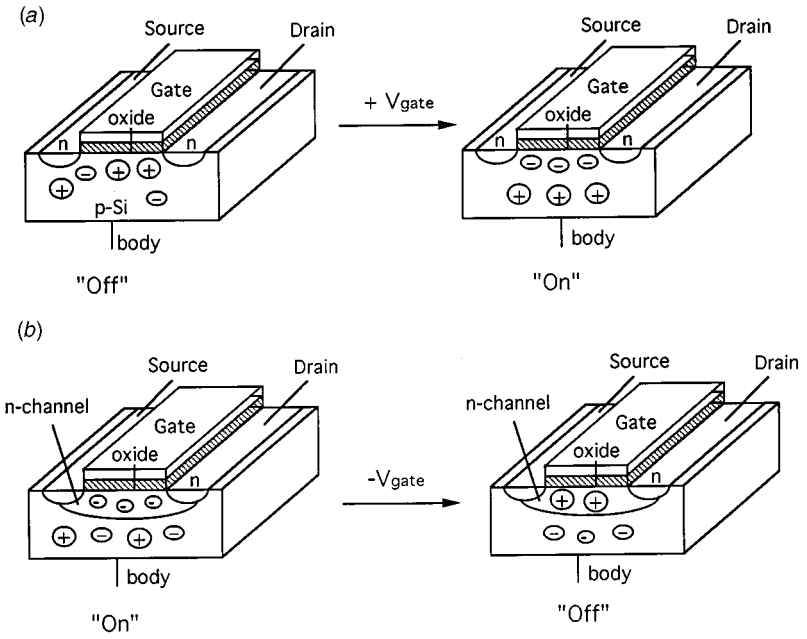

Fig. 2 Schematic illustration of (*a*) an NMOSFET and (*b*) an n-channel MOSFET

electric fields in the channel region. This allows signals to propagate through the computer without losing their strength.

1.3 Scaling problems

MOSFET devices have dominated computer technologies for several reasons including their low operating voltages (0.1 V), low power consumption (low heat), high speed and the ease with which they have been scaled down in dimension. Indeed, in the past MOSFETS could be scaled down simply by shrinking each component part by a constant factor (*i.e.* the channel, source, gate, leads, *etc.*) and operating the device as usual. Unfortunately, it is not at all certain that the operating principles of the MOSFET will scale as the size decreases even below 100 nm. As the n–p–n regions in the transistor shrink, their ability to control the flow of electrons is overcome by the quantum mechanical probability that the electrons simply tunnel through the n–p interface. Furthermore, as the transistor density increases the probability that an electron can tunnel between neighbouring transistors increases. These tunnelling processes cause errors in data manipulation and storage. There is also concern that as the size of a MOSFET decreases, the ability to make any two transistors with the same electronic properties will be lost (*i.e.* achieving a specific dopant density in any two devices will be difficult).[4] The rather obtrusive laws of quantum physics have left researchers with an 'if you can't beat 'em, join 'em' attitude, thus initiating a search for a way to capitalize on quantum effects rather than circumventing them.

2 Single electron nanoelectronics

2.1 Single electron tunnelling: basic theory

The discreteness of charge does not show up at the macroscopic level. Consider, for example, the charging of a large-area capacitor by a battery. The capacitor is charged by displacing electrons from their fixed positively-charged ions on one plate and transferring them to a second plate. The work required by the battery to perform this operation is given by eqn. (1), where

$$W = q^2/2C \tag{1}$$

q is the total charge stored (ne), C the capacitance and e the electron charge.[7] A typical computer capacitor has picofarad (pF) capacitance. If one wanted to charge this capacitor with a single electron, it would be necessary to apply a potential of $V_{ext} = e/2C \approx 10^{-8}$ V. Furthermore, in order to avoid thermal effects, the capacitor would have to be cooled to a temperature such that 10^{-8} V $> kT$ (corresponding to a temperature of 0.0005 K!). Conversely, if more conventional potential increments are applied, say 100 mV, then not one, but $q = CV \approx 10^6$ electrons are stored in the capacitor. Importantly, if the capacitor junction was thin enough and a single electron was able to tunnel from one plate to the other, there would be no observable effect on the charging potential V_{ext}. Thus, although electrons are constrained to integer values once the capacitor is charged, the 'granularity' of electrons is not apparent in macroscale devices.

If the junction capacitance is small ($< \sim 10^{-18}$ F) and the resistance is high, however, the charging energy and tunnelling of single electrons in the circuit can affect the current–voltage (I–V) characteristics of the capacitor.[5] Consider the device shown in Fig. 3(*a*) consisting of a bulk metal–insulator–nanocluster–insulator–bulk metal double tunnel junction (MINIM). (We use the terms cluster and particle interchangeably throughout the review to describe both semiconductor and metal particles less than ~ 50 nm in diameter). When the MINIM is biased by an external voltage source, an extremely unusual current response is observed as the nanocluster capacitor is charged. Current steps are observed separated by voltage plateaus which may span hundreds of mV ('the Coulomb staircase', Fig. 4). Each current step corresponds to the addition of a single electron to the cluster. Below, the models and equations which describe this I–V behavior are examined and their consequences for future electronic device technologies are highlighted.

In the semiclassical approach the MINIM device is treated as two capacitors with capacitances and resistances C_1, R_1 and C_2, R_2 placed in series and driven by an ideal voltage source, V_{ext} [Fig. 3(*b*)]. (The term ideal is used to describe a battery with zero internal resistance which can deliver charge instantly). The state of the system is described by the voltage drop across each junction (V_1, V_2) and Q_0, the number of electrons on the cluster, all classical variables. The dynamics of the system are then determined by the probabilities that an electron will tunnel across junction 1 and/or junction 2, thus altering Q_0 (*i.e.*, a stochastic approach). These tunnelling events are dependent on the change in energy of each electron as it tunnels from the bulk metal through junction 1 and onto the cluster.

To quantify this dependence, consider what happens to a MINIM device upon contacting the two metal electrodes but before an external bias is applied. The Fermi levels of the two bulk metal electrodes and the nanocluster will try to align by tunnelling electrons from the electrodes to the cluster. In general, the Fermi levels will not be able to align exactly but will be offset in energy by one electron or more because of the discrete nature of charge and any impurities present in the junction region. We will ignore these details for now and consider the case of perfect alignment. One further initial assumption is that the quantum mechanical energy levels are closer in energy than the electrostatic energy levels. Now that the system is in electrostatic equilibrium, a potential is applied by the voltage source and n electrons tunnel through the thin insulating barrier and onto the cluster. Our goal is to find n as a function of the applied potential (or applied energy). To describe this process energetically, we focus on junction 1 alone (the local view) seeking the quantity $\Delta E_1 = E_f - E_i$ where ΔE_1 is the difference in the energy of junction 1 before (E_i) and after (E_f) the electron tunnels. This quantity represents the energy that must be supplied by the external voltage source to place an electron on the cluster. The initial state is the energy of junction 1 charged by n electrons [Fig. 3(*c*)]. This energy is given by eqn. (2), where $C_T = C_1 + C_2$ is the total cluster capacitance. Note

$$E_i = (ne)^2/2C_T \tag{2}$$

that C_T is not the circuit capacitance [$1/C_T = 1/C_1 + 1/C_2 = (C_1 + C_2)/(C_1C_2)$] but is the capacitance an electron 'sees' when tunnelling across the first junction. Global views in which the entire circuit capacitance is considered result in identical energy equations.[5] The final state energy, E_f is the energy of the system with an electron on the cluster. Placing an electron on the cluster lowers the potential across V_1 which causes a polarization charge to flow through the circuit. Consequently, the battery does work eV_1 to bring an electron from metal electrode 2 to electrode 1. Combined with the energy associated with changing the cluster charge by one electron one obtains eqn. (3).

$$E_f = eV_1 + [(Q_0 - e)^2/2C_T] \tag{3}$$

Upon expanding term 2 in eqn. (3) and subtracting eqn. (2), we obtain eqn. (4).

$$E_f - E_i = eV_1 - (Q_o e/C_T) + (e^2/2C_T) \tag{4}$$

Note that the energy of the system is fully described by the change in the cluster charge and the work done by the voltage source. To calculate the external voltage that must be applied by the battery or potentiostat, a relation between V_1 and V_{ext} is needed. This is obtained using Kirchoff's loop laws and charge conservation. First, note from charge conservation that eqn. (5) holds.

$$C_1V_1 = C_2V_2 \tag{5}$$

From Kirchoff's laws we obtain eqn. (6).

$$V_{ext} = V_1 + V_2 \tag{6}$$

Combining eqns. (5) and (6) yields eqn. (7),

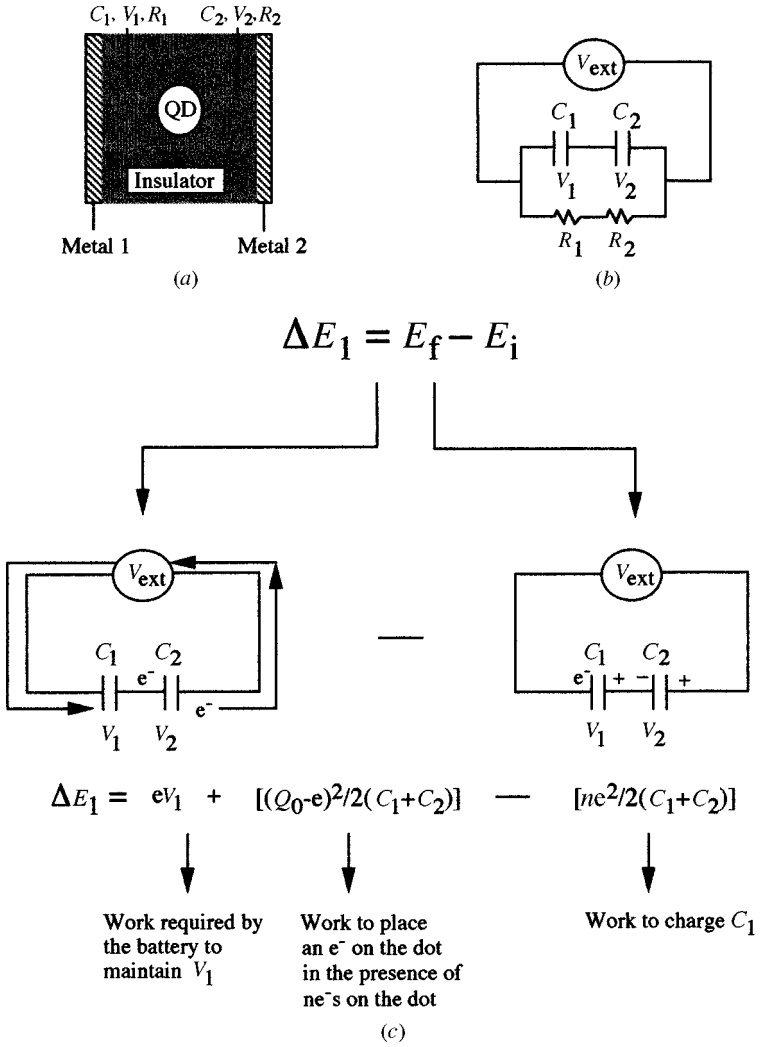

Fig. 3 (*a*) Schematic diagram of a metal–insulator–quantum dot–insulator–metal (MINIM) device; (*b*) an equivalent circuit diagram for the MINIM; (*c*) the equations and equivalent circuit representations which describe the single electron charging and tunnelling events in a MINIM.

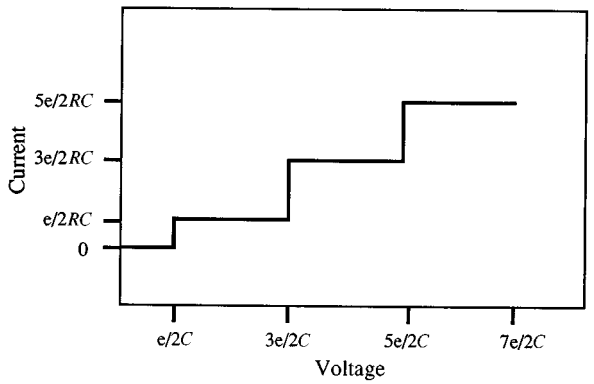

Fig. 4 Schematic depiction of the *I–V* behaviour of an ideal MINIM.

$$V_1 = C_2V_{ext}/C_T \quad (7)$$

and finally eqn. (8).

$$\Delta E_1 = (eC_2V_{ext}/C_T) - (eQ_o/C_T) + (e^2/2C_T) \quad (8)$$

Close examination of eqn. (8) reveals that the first term is the work performed by the voltage source to maintain V_1 after an electron has tunnelled to the cluster. Terms 2 and 3 represent the single electron charging effects. Term 2 is the additional work required to tunnel an electron to the cluster if electron(s) are already present on the cluster. This term provides the voltage feedback necessary to prevent the tunnelling of more than *n* electrons to the cluster per voltage increment where *n* is the step number (*e.g.* $1e^-$, $2e^-$, *etc.* in Fig. 4). In contrast to the macroscale capacitor, where the tunnelling of a single electron would not be noticed, the transfer of a single electron through a nanoscale capacitor causes a substantial energy change in the circuit. This prevents more than the allowed number of electrons (*n*) from residing on the cluster simultaneously.

The current staircase shown in Fig. 4 can now be rationalized by considering the allowed voltage change of the junction, $\Delta V > 0$. If this were not the case the electron would immediately tunnel back to where it came from. Thus eqn. (9) holds.

$$V_{ext} > Q_0/C_2 - e/2C_2 \quad (9)$$

In the case of an initially neutral nanoparticle ($Q_0 = 0$), an external voltage of $e/2C_2$ is required before current may flow through the circuit (the Coulomb gap, or blockade). When this voltage is reached a single electron tunnels to the cluster. The electron does not remain on the cluster indefinitely but quickly tunnels off through the next junction (*ca.* 100 ps depending on the ratio R_2C_2/R_1C_1). It does remain long enough, however, to provide the voltage feedback required to prevent additional electrons from tunnelling simultaneously to the cluster. Thus, a continuous 1 electron current of $I = e/2R_2C_T$ flows through the circuit (notice that e/RC contains units of charge per time). Each additional electron placed on the cluster requires a full e/C_2 in voltage. This leads to the overall 1/2, 3/2, 5/2, *etc.* voltage

increments in the current staircase in Fig. 4 (with each current step after the first of magnitude e/R_2C_T).

A number of important assumptions regarding eqns. (1)–(8) must be emphasized at this point. (i) The only electron transfer events considered were from the electrodes to the nanocluster. Other tunnelling pathways, such as those from electrode 1 to electrode 2 between particles, were not considered. (ii) The voltage source was assumed to deliver charge as fast as the electron tunnels but the time between tunnelling events was long. (iii) Misalignments in the Fermi level due to charge offsets or impurities were not considered. These can be accounted for simply by adding a voltage offset term to eqn. (8). (iv) The quantum mechanical energy level spacing was assumed to be smaller than the electrostatic energy spacing. This assumption is valid for metal particles > *ca.* 5 nm in diameter. Semiconductor particles display quantum effects at sizes much greater than this, however. These effects have been treated successfully within the context of the above models. (v) Tunnelling from one metal electrode onto the nanocluster was considered exclusively. The opposite case, tunnelling from the cluster to the metal electrode, occurs by reversing the applied bias. This results in the identical staircase structure with current steps of opposite sign. Finally, (vi) the resistances of the junctions are so large ($R > h/e^2$) that the electrons are localized on one side of the junction or the other.

In addition to the assumptions stated above, a number of subtleties exist which make the experimental observation of the Coulomb staircase challenging. One challenge is in designing a system with optimum junction capacitances and resistances. Simulated MINIM *I–V* curves show that the sharpest steps are observed for C_2 and $R_2 \gg C_1$ and R_1 [Fig. 5(*a*) and (*b*)].[8] As C_2/C_1 and R_2/R_1 approach 1 the zero-current plateau at 0 V remains but the current steps disappear. This represents a departure from assumption (ii) above. If R and C for the two junctions are equal the electron will tunnel through both junctions with identical rates. The voltage feedback required to see current steps is thus lost. Unfortunately, since C decreases but R increases as the junction thickness increases, these ratios can only be optimized by constructing the two junctions from materials with different dielectric properties.

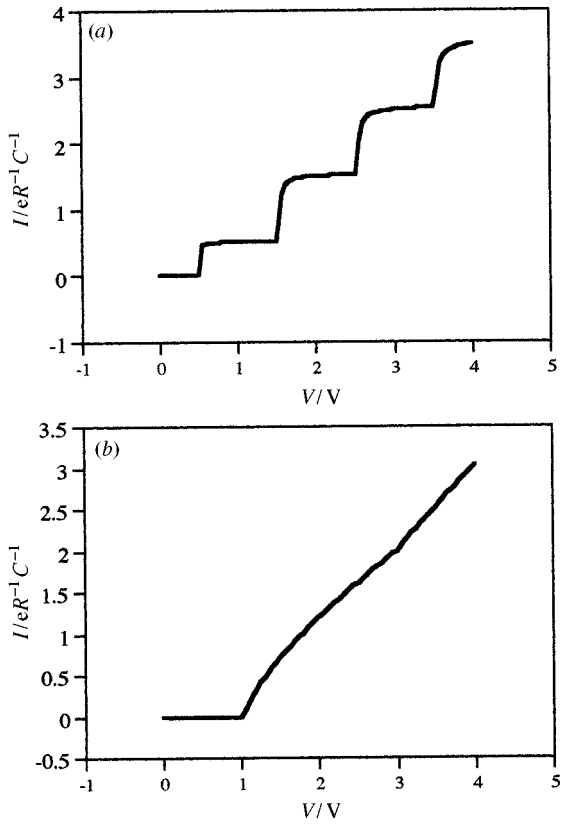

Fig. 5 Calculated *I–V* curves for a MINIM with (*a*) C_2/C_1 and $R_2/R_1 = 100$ and (*b*) C_2/C_1 and $R_2/R_1 = 1$. Both plots assume $e^2/C_T \gg kT$.

The biggest obstacle to designing a MINIM device was mentioned briefly above—that is, thermal effects. To avoid thermally-activated tunnelling processes, $e/2C_2 \gg kT$. As T increases the single electron current steps are gradually washed out and an ohmic response (linear *I–V* curve) is observed. The room temperature operation of single electron devices is therefore limited to clusters < *ca.* 12 nm in diameter.

Finally, we must point out that many experimental configurations involve measuring the *I–V* properties of parallel arrays of clusters [*e.g.* metal–insulator–$(\text{nanocluster})_N$–insulator–metal devices, see Section 3.2]. The arguments above hold for these systems with the exception that the current steps are of magnitude Ne/RC. In other words, each cluster acts as a single MINIM with their currents additive. An additional challenge to the observation of Coulomb charging effects in these systems is that the dispersity in the diameter of the clusters must be low. Otherwise the varying capacitances (and charging energies) of the nanoclusters will cause the steps to blend together and the *I–V* curve will again appear ohmic.

An interesting analogy to the behaviour of MINIM devices has been drawn by Kastner.[9] He has used the term 'artificial atom' to describe the controlled addition of single electrons to nanoparticles. In the analogy, adding electrons to a particle is similar to adding electrons to an atomic nucleus in moving across a row of the Periodic table. If a gate electrode is included in the structure, the analogy can be stretched further. A positive gate bias pulls charge away from the cluster allowing excess electrons to tunnel from the source to the cluster. The gate electrode can thus be used to control the number of extra electrons on the dot. This is equivalent to adding protons to an atom. Of course, adding positive charge to a nucleus changes the number of electrons that must reside on a neutral atom. In fact, the analogy does have a mathematical foundation. The potential energy of a two-particle system (the hydrogen atom) is $-1/4\pi\varepsilon_0(e^2/r)$ and the capacitance of an isolated sphere is $4\pi\varepsilon_0 r$ (r is the sphere radius). Combining these terms yields the energy of a hydrogen atom in terms of its capacitance. Conversely, the energy of a hydrogen-like nanoparticle 'atom' is obtained. This is eqn. (2) above.

2.2 Single electronics: a brief history

Predictions of single electron charging effects date back to the 1950s.[10] Soon after, the existence of the Coulomb blockade of electrons was demonstrated for electron hopping in granular metal films.[11] It was not until 1987, however, that broad current steps were observed in the low-temperature (4 K) *I–V* curves of Cu–Al_2O_3–sputtered Ag island–Al_2O_3–Ag sandwich structures.[12] The 'smearing' out of the steps was attributed to polydispersity in the size of the Ag islands. Sharper current steps were revealed by Ammen and coworkers when the tip of a scanning tunnelling microscope (STM) was placed over a single Au island.[13]

During this time, experiments were also being performed on devices fabricated lithographically. In pioneering experiments, Fulton and Dolan fabricated spatially well-defined MINIM double tunnel junctions in which a gate electrode was placed near the central island.[14] These workers showed that charging effects could be modulated by applying a gate bias. This three-terminal device, by analogy to the MOSFET described above, was named a single electron transistor (SET). The flow of single electrons from source to drain in the SET was controlled by injecting (or removing) single electrons from the metal dot through the gate lead. Once again, however, because of the large size of the device, these experiments were performed at extremely low temperatures (1 K).

The fundamental experiments described above provided important evidence that single electron tunnelling effects

existed and gave hope that SETs might one day form the basis of advanced computing devices. At this point, however, an impasse was reached with regard to the fabrication of Coulomb blockade devices. On one hand, photolithographic techniques were capable of fabricating complex SET structures easily and cheaply, but with minimum size features of only *ca.* 100 nm. This limited the operation of SETs to sub-Kelvin temperatures. (Likewise, electron beam lithography, while capable of producing features of the order of 5 nm, is expensive, slow and still not readily available.) On the other hand, relatively simple metal evaporation methods provided metal islands with features down to 10 nm, but the precise placement and dispersity of the islands was difficult to control. In contrast to lithography and metal evaporation, wet-chemical synthesis can provide clusters of almost arbitrary size. This has prompted research aimed toward single electron devices which assemble themselves from solution.

3 Self-assembled single electron tunnelling devices

3.1 Synthesis and self-assembly of colloidal particles on solid surfaces

For the purposes of this review, self-assembly is defined as the solution phase chemically directed organization of materials into pre-designed composite structures. The composite structure of interest here is the MINIM, containing a metal or semiconductor nanoparticle < 20 nm in diameter.

Chemically-synthesized nanoparticles offer several advantages as SET components, most important of which is their small size. Metal and semiconductor nanoparticles can be prepared in solution with average diameters tens of Ångstroms and larger. Adsorbed or covalently attached ligands can act as stabilizers against agglomeration and can be used to impart chemical functionality to nanoparticles. Importantly, nanoparticles can be immobilized between insulating thin films through electrostatic or covalent attachment chemistries.

Countless methods for synthesis of metal and semiconductor particles have been published; these have been reviewed elsewhere.[15,16] For example, II–VI semiconductor nanoparticles (CdS, ZnS) have been prepared by introducing H_2S or Na_2S into a solution containing the appropriate cation ($ZnCl_2$, $CdCl_2$) or by pyrolysis of organometallic precursors (alkylcadmium, silylchalcogenides) in hot coordinating solvents (tri-*n*-octylphosphine).[17] Colloidal metals are typically made by addition of a reducing agent (citrate, $NaBH_4$) to a solution of the metal salt ($HAuCl_4$, H_2PtCl_4); the smaller metal clusters ($\lesssim 3$ nm) are often prepared by gas phase or liquid two-phase systems containing 'capping ligands' (RSH). Capping ligands or surfactants can be used to stabilize the nanoparticles and prevent the formation of larger particles and agglomerates. The capping ligand : metal ratio is used to control the final cluster size. While methods for preparing colloidal particles are numerous, the goal of producing monodisperse clusters of a target diameter has been attained only in a few cases, most notably Au. Au nanoparticles can be prepared with mean diameters from 0.84 to more than 200 nm.[15] In fact, many sizes are commercially available (Nanoprobes, Goldmark Biologicals).

The stability and reactivity of colloidal particles is determined largely by the ligand shell adsorbed or covalently bound to the surface of the particle. Nanoparticles tend to aggregate and precipitate; this can be prevented by the presence of a ligand shell. Water-soluble sulfonated phosphine ligands [P(*m*-$C_6H_4SO_3Na)_3$] have been used to stabilize CdS and Au nanoparticles. The phosphine-stabilized particles can be isolated and resuspended without agglomeration. Unfortunately, these ligands degrade slowly in the presence of H_2O or O_2, limiting their long-term stability.[16] Recently, Brust and coworkers prepared ligand-stabilized Au clusters from a two-phase solvent system containing $C_{12}H_{25}SH$. These clusters exhibit solubility in organic solvents, can be evaporated to dryness and resuspended, and are air stable.[18] Since this work was first published, several groups have shown that bifunctional organothiol ligands ($RC_nH_{2n}SH$, where R = Br, CH_2=CH, ferrocene, *etc.*) can be used to control the surface chemistry and reactivity of Au nanoparticles.[19,20] The capping ligand may then be employed in coupling reactions to produce more complex assemblies. An elegant example of this was provided recently by Alivisatos and coworkers who reactively coupled SH–terminated single stranded DNA oligonucleotides to maleimido-funtionalized 1.4 nm Au clusters.[21] Upon addition of complementary oligonucleotides, these particles self-assembled to form dimers and trimers. In similar work, Mirkin and coworkers prepared 3D superstructures of 13 nm Au colloids capped with SH-terminated DNA nucleotides.[22] Such directed assembly using chemically-functionalized ligand shells holds great potential for control and direction of nanoparticle placement in device fabrication.

Construction of electronic devices such as SETs requires the assembly of nanoparticles onto solid supports. Solution-based approaches to surface assembly of metal and semiconductor nanoparticles typically involve electrostatic or covalent binding of the particle to a surface-bound molecular or polymeric thin film. For example, surfactant structures (monolayers, bilayers, *etc.*) have been used to direct assembly of metallic, semiconducting and magnetic particles.[23] This can be accomplished by adsorbing particles electrostatically to charged surfactant headgroups, or by *in situ* generation of particles beneath monolayers at the air–water interface. Surfactant monolayers with or without attached nanoparticles can be transferred to solid supports using standard Langmuir–Blodgett techniques. Nanoparticles can also be assembled on solid supports using polyelectrolytes. Schmitt *et al.* and Mallouk *et al.* have prepared multilayered insulator–Au particle–insulator structures with alternating anionic and cationic polyelectrolyes as the insulating layers.[24,25] The thickness of the polyelectrolyte layers between particles was varied by increasing the number of cation and anion deposition cycles (see Section 3.2).

Covalent attachment strategies often take advantage of the reactivity of the outer shell atoms in the cluster. Many metallic and semiconducting clusters (Au, Ag, CdS, CdSe) have a high affinity for amine and/or thiol moities. For example, Alivisatos and coworkers have covalently attached CdS particles to bulk Au and Al substrates using bifunctional crosslinkers (dithiols, thioglycolate).[20] Natan and coworkers have assembled Au and Ag colloidal particles on NH_2- and SH-terminated organosilane polymers on SiO_x and SnO_2 substrates. The kinetics of this surface-assembly reaction have been investigated in some detail, affording control over the number of particles on the surface.[26] Alternatively, close-packed monolayers of alkanethiol stabilized clusters have been formed by solvent evaporation.[18,27] In this case, the length of the organic ligand defines the distance between particles. This distance has a pronounced effect on the electronic properties of the resulting 2D array (see Section 3.2). Recently, lines and grids of Au particles have been fabricated with features less than 1 μm by combining Au self-assembly with microcontact printing[28] or conventional lithography techniques.[29]

Using wet-chemical approaches to nanoparticle organization, such as those described here, one can envision assembly strategies for nanoparticles of nearly any material on almost any substrate. The versatility of these immobilization methods makes it possible to design a number of self-assembled electronic devices including the insulator–cluster–insulator tunnel junction of the SET. Despite these recent advances, numerous challenges remain in the area of nanoparticle synthesis and assembly. Control over size, monodispersity or ligation is not currently available for most metal and semiconductor materials in the size range of interest for SETs (< 12 nm). Increasing the monodispersity of nanoparticles would improve the operation of single electron devices. In addition, methods for arranging nanoparticles into more complex 2D and 3D

assemblies (other than submonolayers and simple closest-packed geometries) are completely lacking. A self-assembled 2D square lattice of clusters, for example, would be an interesting analogue of large 2D arrays which have been fabricated lithographically.

3.2 Current–voltage characteristics of self-assembled single electron devices

Andres and coworkers have investigated the *I–V* properties of self-assembled Au nanocluster films extensively. In one type of experiment, 1.9 ± 0.6 nm diameter Au clusters were bound to a bulk Au substrate *via* a SAM of the dithiol *p*-xylene-α,α′-dithiol (XYL dithiol).[27] An STM tip was placed over a single nanocluster to complete the Au–dithiol–Au nanocluster–air gap–STM tip double tunnel junction. *I–V* measurements revealed a Coulomb gap and one clear current step at positive bias even at room temperature. A number of important electrical parameters were also ascertained from their data. For example, the resistance of a single XYL molecule was estimated to be 18 ± 12 MΩ and the dithiol junction capacitance was estimated to be 1.7×10^{-19} F. These values agreed well with theoretical predictions.

In a second type of experimental arrangement, Andres and coworkers assembled a 2D array of decanethiol-coated Au nanoclusters between two Au electrodes separated by ~450 nm.[27] Coulomb blockade effects were again marked by the appearance of a high resistance gap around 0 V in the *I–V* curves. Interestingly, when the nanoclusters were exposed to a conjugated aryl diisonitrile molecule, the *I–V* response became ohmic. Presumably, this was due to a combination of increased electronic overlap between particles resulting from the π system of the conjugated molecules and the distance dependence of electron hopping between Au centres (the Au–Au distance increased by 0.4 nm as the diisonitrile bound).

Experiments similar to those described above were conducted by Murray, *et al.*[19] In their work, Au clusters stabilized by alkane thiol SAMs of varying alkyl chain lengths (C_8, C_{12}, C_{16}) were assembled across the gaps of interdigitated array electrodes and investigated electronically. Non-linear *I–V* curves were reported for these systems which depended on the length of the alkane chain. Conductivities of the 2D arrays calculated from the *I–V* curves revealed a two order of magnitude decrease for every four carbons in the alkane chain. Murray pointed out that the *I–V* properties observed in Au cluster monolayers in the high potential limit fit well to models usually employed in interpreting electron transfer in redox polymer systems. These models provide additional insight into the Au cluster–cluster electron transfer mechanism, rate, coupling coefficient and charging energy.

Mallouk and coworkers have used a combination of layer-by-layer inorganic polyelectrolyte and Au nanocluster self-assembly methods to fabricate MINIM devices.[25] This scheme is depicted in Fig. 6. First, a clean bulk substrate was immersed in a solution of mercaptoethylamine hydrochloride to immobilize cationic sites on the surface. The substrate was then alternately soaked in aqueous solutions containing single anionic sheets of lamellar inorganic solids [$KTiNbO_5$, α-$Zr(HPO_4)_2 \cdot H_2O$ (ZrP)] and organic polyelectrolyte cations [polyallylamine hydrochloride (PAH)]. A 'monolayer' of the desired polyelectrolyte ion exchanges onto the oppositely-charged material deposited on the substrate during the previous immersion step (*i.e.* anionic ZrP to cationic PAH). Multilayers of the same material cannot form on the surface during a single immersion step because of electrostatic repulsion. The thickness of the resulting film was thus defined by the number of immersion cycles the substrate was subjected to. Once the desired junction thickness was assembled, Au nanoparticles were introduced into the film by soaking the substrate in a solution containing citrate-stabilized Au nanoclusters. Au colloids bind readily to the amine functionalities contained in PAH. Following Au cluster deposition, a second insulating junction was formed by simply reversing the adsorption sequence used to form the first junction. Note that the two junctions may be designed to vary in thickness and/or composition (*i.e.* a different inorganic may be chosen for junction 2). A thin layer of the organic conducting polymer poly(pyrrole) was polymerized on top to complete the MINIM device.

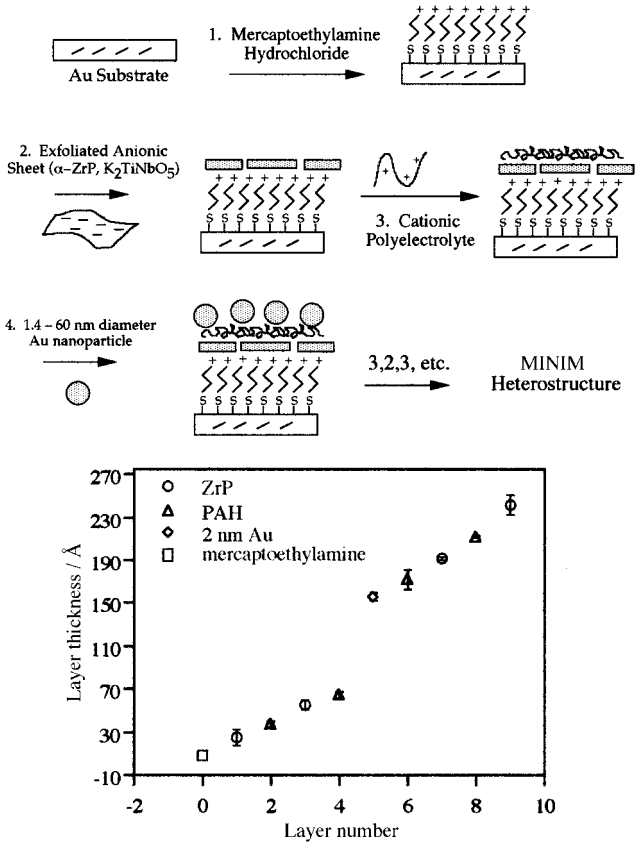

Fig. 6 Illustration of the polyelectrolyte sequential adsorption route to MINIM devices developed by Mallouk and coworkers. The plot at the bottom shows ellipsometry data of layer thickness *vs.* layer number for a typical device (see ref. 25 for details).

I–V curves of MINIM devices fabricated with 2.5 ± 1.5 nm diameter Au nanoclusters displayed Coulomb gap potentials at room temperature which agreed well with predictions based on eqn. (9). The magnitude of the gap potential was somewhat tunable *via* the junction thickness; decreasing the junction thicknesses from 80–30 Å (by decreasing the number of polyelectrolyte pairs) decreased the Coulomb gap potential from 400 to 275 mV. In addition, changing the Au nanocluster size also affected the *I–V* properties of these devices. Fig. 7 shows a series of *I–V* curves recorded at various temperatures for a device fabricated with 12 nm diameter Au clusters. At temperatures close to 25 °C, an ohmic response was observed because the capacitance of the particles was such that $kT > e/2C$. Upon cooling slightly, however, the *I–V* curves became increasingly non-linear as the single electron charging energy began to dominate the tunneling process.

Although single electron current steps were not observed in these devices (probably because $C_2/C_1 = 1$), the inorganic polyelectrolyte self-assembly approach appears to be a promising route to MINIM devices since (i) lamellar inorganic solids with a wide range of dielectric properties are amenable to the assembly methods outlined above (providing a means of optimizing C_1 and C_2) and (ii) defects do not seem to be a concern. Note that single electron charging effects were observed in devices consisting of a parallel array of $\sim 10^{11}$ clusters covering large areas (1–2 cm^2). This indicates that the

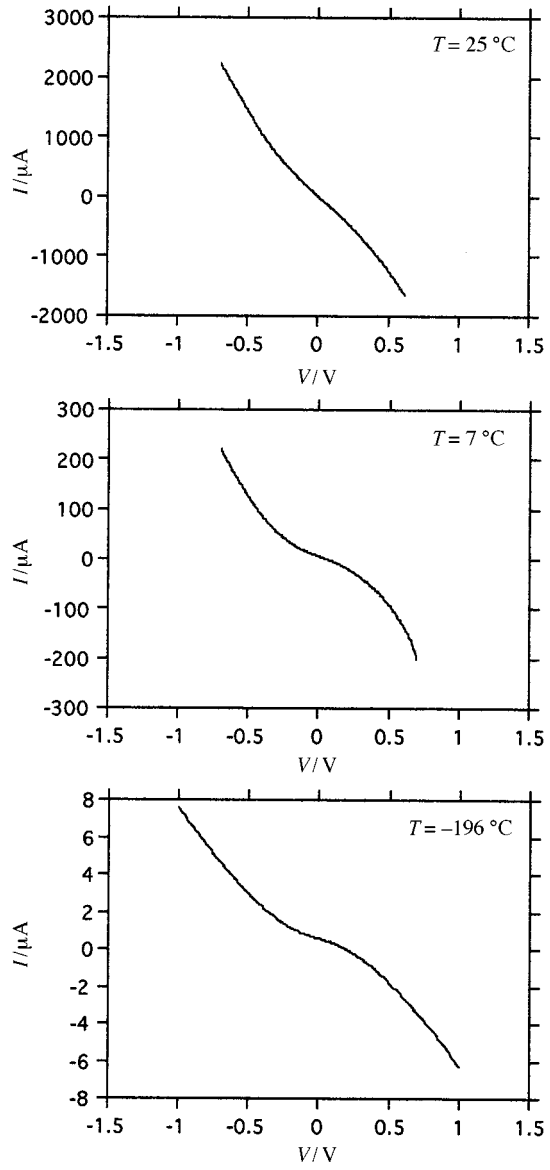

Fig. 7 *I–V* curves at three temperatures for a MINIM device consisting of an Au substrate–60 Å ZrP/PAH–12 nm Au nanoparticle–70 Å ZrP–PAH–poly(pyrrole).

devices do not short-circuit themselves through defects. Scaling the device down in size by assembling the films on pre-patterned surfaces should therefore be straightforward and will only diminish the defect density.

A self-assembled MINIM structure was recently scaled down to the level of a single particle by Alivisatos, McEuen and coworkers.[30] To fabricate the structure, a combination of optical lithography and angle evaporation techniques were first used to define a narrow gap (a few nm) between two Au leads on a Si substrate [Fig. 8(*a*)]. The substrate was then placed in an isopropyl alcohol solution containing hexane-1,6-dithiol. The dithiol binds to Au surfaces linearly, with one end attached to the surface and the other end facing the solution. The free end was used to assemble 5.8 nm Au or CdSe clusters in the region between the leads [Fig. 8(*b*)]. A Au–dithiol–nanocluster–dithiol–Au device resulted from these procedures. An *I–V* curve for a device with a 5.8 nm Au cluster displaying slight current steps is shown in Fig. 9. Fitting the curve to the Coulomb blockade models presented above gave C_1 = 2.1 aF, C_2 = 1.5 aF, R_1 = 32 MΩ and R_2 = 2 GΩ.

While it is unclear why the same dithiol linker would result in two junctions with such different capacitances and resistances,

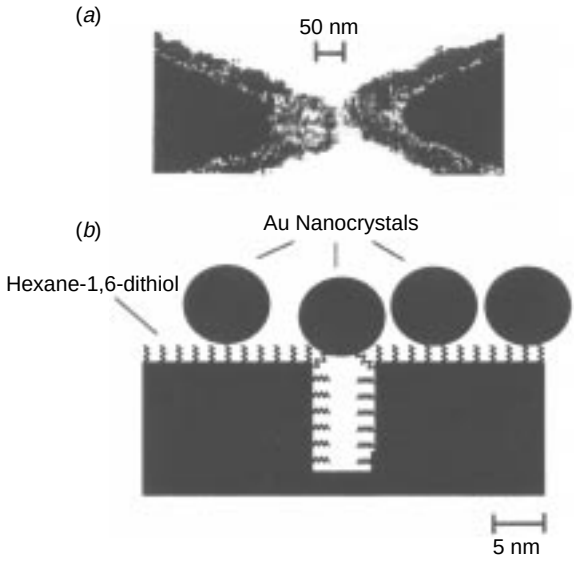

Fig. 8 (*a*) Field emission scanning electron micrograph of a lead structure prior to the assembly of nanocrystals; (*b*) schematic cross section of nanocrystals bound to the leads. (Taken from ref. 30).

this approach to single electron devices is exciting in part because the gate electrode is built-in. The underlying Si substrate was used recently as a gate to externally control the flow of single electrons from source to drain to make a true SET.

Recent work by Moskovits and coworkers, while probably not self-assembly in the strictest sense, deserves mentioning.[31] Moskovits used porous Al_2O_3 membranes as a template for the synthesis of metallic and semiconductor wires. Membranes with pore diameters ranging from 4 to 250 nm have been synthesized by oxidizing an Al substrate in acidic media. The underlying Al can then be used as the working electrode for the electrochemical deposition of a number of metallic, magnetic and semiconductor materials. For example, Ni wires were electro-deposited in the pores of a 10 nm diameter porous membrane and the Ni was oxidized at the tips. Sputter-depositing Ag on top resulted in a Ag–NiO–10 nm Ni wire–Al_2O_3–Al MINIM device [Fig. 10(*a*)].

I–V curves for the template-synthesized MINIMs show remarkably well-defined current steps [Fig. 10(*b*)]. Interestingly, each voltage plateau is of the same magnitude (~1 V). Recall from the discussion above that the first current step should require half the voltage of each successive step. This observation, and the large background current associated with each step, is likely a consequence of electronic coupling between the closely spaced wires. (Each wire was separated by approximately 10–20 nm.) The electronic coupling between wires effectively adds an additional charging term to eqn. (9) and can shift the entire *I–V* curve up and to the right (Fig. 11). Similar effects were briefly noted for a gate bias or impurity

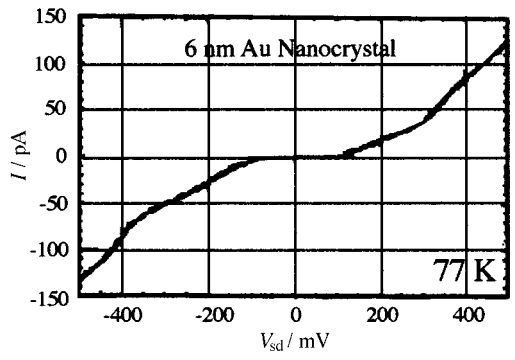

Fig. 9 *I–V* characteristic of a 5.8 nm diameter Au nanocrystal measured at 77 K. (Taken from ref. 30).

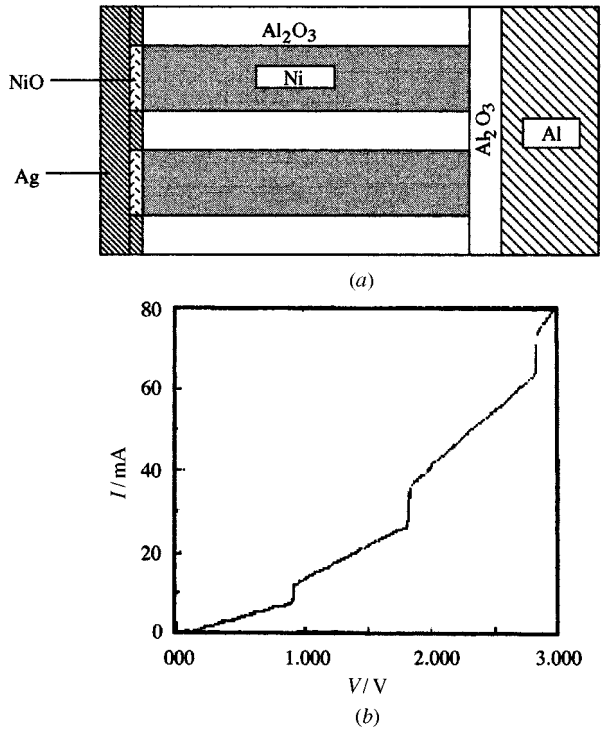

Fig. 10 (*a*) Schematic diagram of a 10 nm diameter MINIM fabricated in the pores of an anodically-etched Al_2O_3 film; (*b*) *I–V* characteristic of the device depicted in (*a*) showing several current steps as a function of potential. (Taken from ref. 31, copyright 1996, IEEE).

charge in section 2.1. These experiments illustrate the importance of the local environment for the electronic properties of single electron devices.

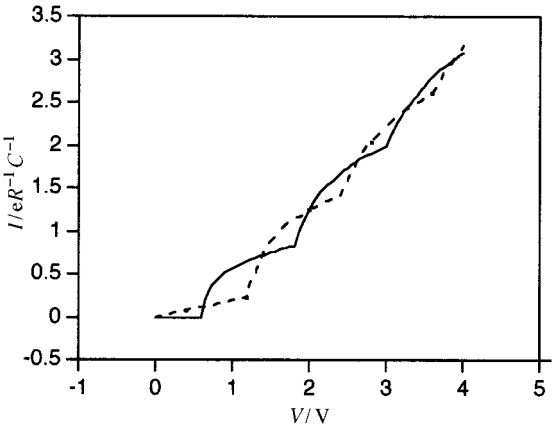

Fig. 11 Calculated *I–V* curve for a MINIM with an initially uncharged particle (solid line) in the presence of an external charge source (dashed line). Both plots assume $e^2/C_T \gg kT$; C_2/C_1 and $R_2/R_1 = 100$.

4 Applications of single electron devices

Numerous applications for single electron transistors have been suggested. These include ultra-high density information storage, supersensitive electrometry, near-infrared radiation receivers and dc current standards.[5] Several applications have already been demonstrated at low temperatures in devices fabricated lithographically. Below, we highlight the operating principles of SETs as they pertain to two of the more advanced applications—computing and electrometry.

4.1 Single electron memory

Perhaps the ultimate application of the SET is as a memory cell in which information is stored as the presence or absence of a single electron on the cluster. Two routes have been suggested for implementing SETs into digital circuitry. The first is to mimic conventional MOS technology. In this scheme, a single electron injected onto the cluster from the gate electrode modulates the source–drain current. As with the MOSFET, current flow (on or off) would represent '1s' and '0s'. Single electron memory of this type was demonstrated independently by Chou and Chan recently.[32,33] Their SETs consisted of a Si nanoparticle (or several particles in Chan's device) embedded in a thin SiO_2 insulator. Conductive Si source, drain and gate electrodes surrounded the particles. Chan's devices displayed read/write times of *ca.* 20 ns, lifetimes in excess of 10^9 cycles and retention times of days to weeks (meaning the charge does not leak out of the dot during this time). Although these are not exceptional quantities, read/write times of ~30 ps are possible in CMOS transistors, they are certainly acceptable when one considers that it may be possible to integrate 4–5 orders of magnitude more SETs cm^{-2} than is viable with the current state-of-the-art transistor. The incorporation of Si cluster devices into existing Si technologies is also appealing.

A second proposed method for utilizing SET-based memory is to make 1 bit = 1 electron rather than using the source–drain dc current flow. As proposed, arrays of typically 4 to 7 SETs are connected in series and the positions of single electrons in the array are used to designate different memory states. This design has been difficult to realize in practice. If successful, however, this type of memory may have advantages over the MOSFET-type memory described above. One advantage could be gained when the time comes for the large scale integration of SETs to form logic gates. Integrated SETs operating on conventional principles may have problems due to their inherently low voltage gain. Coding memory by single electrons rather than voltage signals avoids this problem.

4.2 Supersensitive electrometry

While single electron computing continues to be the ultimate goal of SETs, the most advanced practical application currently for SETs is probably as an electrometer (a device used to measure charge). The SET electrometer is operated by capacitively coupling the external charge source of interest to the gate. Changes in the SET source–drain current are then measured as the unknown charge quantity is placed on the gate. Esteve has reported a charge sensitivity of 600 pA per e^- for an SET electrometer fabricated lithographically.[5] Fulton and coworkers recently built a scanning SET electrometer on the end of a sharp glass tip.[34] Sub-single electron charges placed near the tip caused measurable changes in the SET source–drain current. For example, when placed in close proximity to an illuminated GaAs–AlGaAs heterostructure, individual photo-ionized charge sites in the semiconductor could be mapped across the surface with a resolution of 100 nm. Extremely sensitive capacitance measurements have also been performed using a similar configuration. The SET electrometer is loosely considered to be the charge analogue of the SQUID device used for magnetic flux measurements (although not quite as sensitive).

The SET electrometer is in principle not limited to the detection of charge sites on a surface, but should be applicable to a wide range of sensitive chemical signal transduction events as well. For example, if the nanoparticle of an SET is capped with alkane thiols containing an analyte receptor moiety, the *I–V* properties should be extremely dependent on any binding or redox events that occur at the particle surface (Fig. 12). There are two possible mechanisms which would alter the *I–V* curve upon analyte binding, a change in particle capacitance or charge (in analogy to the scanning SET when it approaches a surface charged surface). It is difficult to predict, *a priori*, the magnitudes of these changes; however, Murray and coworkers have recently employed rotated-disk voltammetry to measure the average capacitance change per particle during the oxidation of ferrocene-terminated alkane thiols attached to Au clusters

(these experiments were conducted on 0.1 mM solutions of Au clusters).[19] The average capacitance increased by a factor of 8 upon oxidation, an extraordinary change considering that only a few molecules on the particle surface were oxidized. Our calculations suggest that in the configuration shown in Fig. 12(*a*), a capacitance change of this magnitude would result in large shifts in the *I–V* curve [Fig. 12 (*b*)]. These calculations demonstrate the potential to detect a redox event occurring on even a single molecule attached to a metal nanoparticle, thus enabling fundamental studies of the kinetics and thermodynamics of single-molecule electron transfer events.

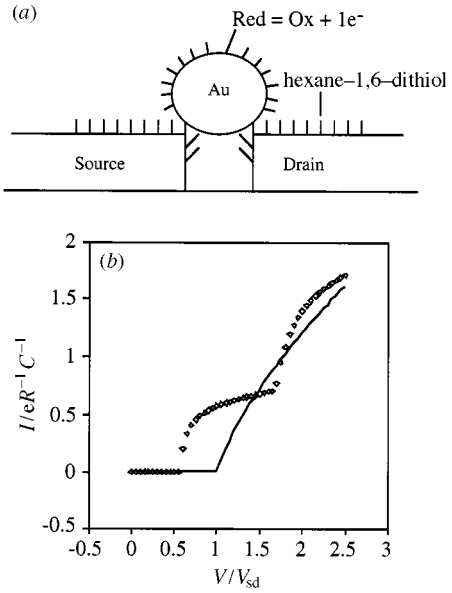

Fig. 12 (*a*) Schematic illustration of a Au nanoparticle assembled between two metal electrodes. The nanoparticle is capped with alkane thiols and a single, generic redox active α,ω-substituted alkane thiol which can undergo the redox reaction shown; (*b*) calculated *I–V* curves for the structure shown in (*a*) assuming an eight-fold capacitance change (see ref. 19) in going from Red (solid curve) to Ox + 1e$^-$ (diamonds).

4.3 Lage-scale integration of SETs

Looking ahead to the all-SET computer one might envisage a number of problems. For example, although 1 SET has demonstrated useful memory capabilities, how will 10^x SETs (with *x* being very large) be integrated? How will the integrated SET systems be connected to the outside world? Chemical self-assembly is in principle an ideal way of solving these problems. Recently, the first steps toward the integration of nanoclusters were taken by Alivisatos. His group synthesized CdSe clusters capped with *N*-methyl-4-sulfanylbenzamide (MBAA). Reaction of the MBAA with bis(acyl hydrazide) crosslinked the particles and CdSe dimers were isolated from the mixture by centrifugation.[35*a*] The DNA-crosslinked Au dimers and trimers described in Section 3.1 constitute a second important milestone in the integration of nanoclusters. We have taken a similar approach to integrated systems by attaching 1.4 nm Au clusters to tetrakis(*p*-aminophenyl)porphyrins. Au–porphyrin dimers (20%) and trimers (5%) were observed in the product mixture (Fig. 13). Au–porphyrin tetramers were not produced, presumably because of steric hindrance. Porphyrins were chosen as the 'scaffolding' from which to build cluster arrays because of their rigidity and well-developed coupling chemistry. In fact, very large porphyrin arrays have been synthesized which could be modified to accommodate metal clusters in the precisely-defined arrangements required for single electronics.

Johnson and coworkers have recently developed an approach to integrating nanoparticle structures whereby Au clusters are linked up directly on a planar surface or between source and drain electrodes.[35*b*] This was accomplished by first adsorbing a single layer of well-spaced 10 nm diameter Au clusters to the surface, treating the particles with hexane-1,6-dithiol and finally, treatment with a second layer of Au clusters. The second layer of Au clusters attached to the first layer *via* the thiol linker, in many cases forming Au cluster trimers, tetramers, *etc.* When applied to source and drain electrodes, this method produced Au cluster trimers which spanned the gap between leads, enabling electronic characterization. Single electron tunnelling was observed for these systems, the capacitances in accord with those observed by Alivisatos.

The question remains as to how the SET arrays will be wired to the outside world. (It is not an unreasonable task to make

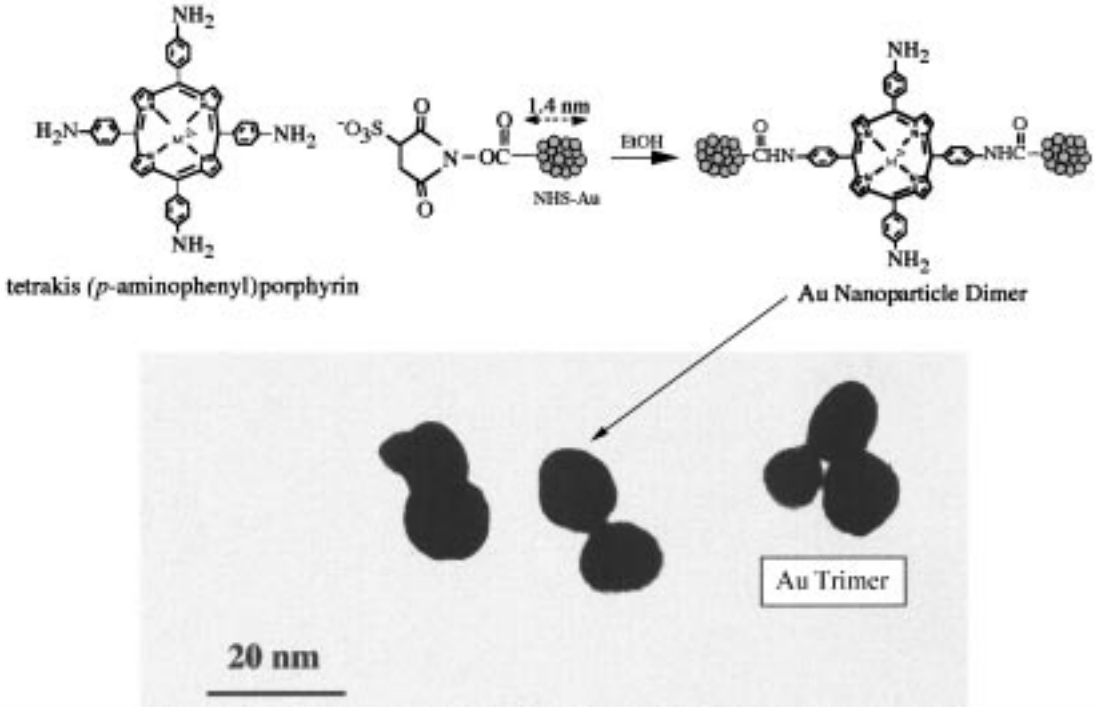

Fig. 13 Transmission electron micrograph showing the Au nanoparticle dimers and trimers which formed as a result of the reaction shown at top. The Au particles were initially 1.4 nm in diameter but were 'enhanced' by selective Ag reduction (Nanoprobes) for better viewing.

electrical connections to a single nanotransistor. Contacting 10^{12} transistors is quite a different demand.) One way to accomplish this may be to employ a hybrid approach where SETs and related devices are integrated together with existing MOSFETs. This approach is appealing because it could increase the integrated circuit density while building on 50 years of existing technology. Notice from the Moore's law plot (Fig. 1) that the era of nanoelectronics would be ushered in more quickly using this strategy.

A second approach, proposed separately by Lent and Korotkov, is to forgo the wires altogether.[4] This scheme, appropriately named quantum cellular automata (QCA), is based on the electrostatic interactions present between cells of connecting clusters. In Korotkov's design, the basic cell is a line of nanoclusters connected by insulating material (Fig. 14, top). An electric field applied in either direction polarizes the string to give a '1' or '0' state. Lent's QCA is similar in principle, but square cells of nanoclusters carry the polarization states (Fig. 14, bottom). Again, two states are possible depending upon the direction of the applied field. In either design the cells are connected in various configurations to make more complex logic circuits. Fig. 15 illustrates how Lent's cells are connected to form a logic gate. The dark and open circles correspond to one-electron rich and one-electron deficient clusters, respectively. Note that the configuration of the overall circuit provides a vehicle for controlling the polarization state of individual cells (*i.e.* the entire circuit relaxes to its low-energy configuration). Alternating 1s and 0s result from the design shown in Fig. 15.

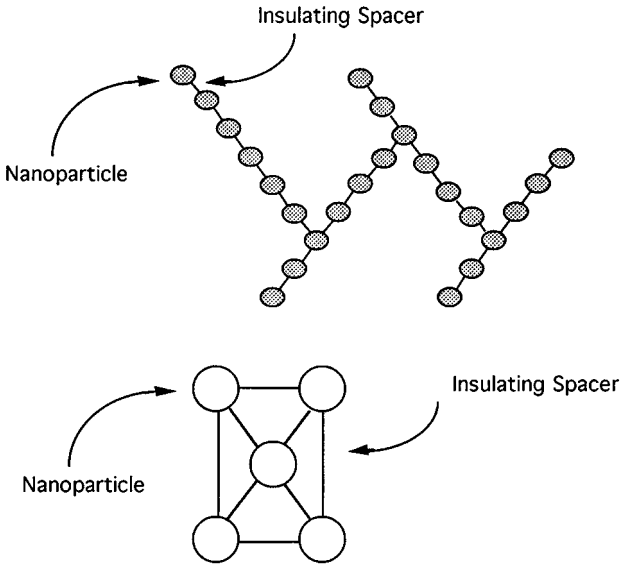

Fig. 14 Nanoparticle–insulator structures proposed in the wireless computing schemes of Korotkov (top) and Lent (bottom).[4] The circles represent quantum dots, the lines are insulating spacers.

The advantage that QCA offers over conventional circuit technology is that signals are rapidly transferred between interconnecting cells *via* electrostatic interactions only. These signals travel at the speed of light, so the time required for one cell to influence another is negligible. Furthermore, electrostatic signals can be transmitted over long distances, making communication between large arrays of cells possible without extensive wiring. This advantage, along with the small size of each cell (as low as ~ 2.5 nm^2), makes the prospects of ultra-high density data storage excellent.

A four-dot QCA logic cell was recently demonstrated by Lent and coworkers.[4b] Their device, fabricated lithographically, consisted of four Al islands situated at the corners of a square with Al_2O_3 serving as tunnel barriers between islands. Gate electrodes were used to switch the single-electron polarization states, trapping electrons on specific islands for periods of

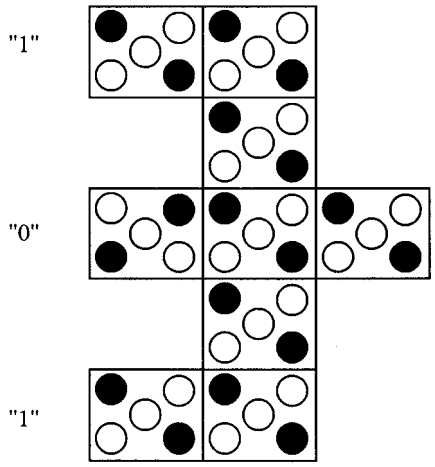

Fig. 15 A simple logic circuit consisting of an array of individual quantum dot cells as described by Lent and coworkers.[4] The dark and open circles represent quantum dots with an excess and deficiency of charge, respectively.

minutes. Although the device was much larger (8 μm) than current MOSFETS and operated at much lower temperatures (1 K), this work demonstrated QCA logic for the first time experimentally.

Two important factors must be considered in designing more complicated QCA structures. First, one must consider that when relying on electrostatics to set up a memory state the location and size of each dot must be controlled precisely. Deviations from a particular structural design will lead to undesirable tunnelling events and, hence, data manipulation errors. Second, as with the SET, if QCA is to function at room temperature the islands must be < 10 nm in diameter. In this respect, Au–porphyrin or Au–DNA building blocks may prove useful for the solution-assembly of QCA circuits that operate at much higher temperatures than devices fabricated lithographically.

5 Summary and future challenges

If Moore's first law states that integrated circuitry roughly doubles in density every 18 months, his second law might be that the cost associated with the first law quadruples every 18 months. If integrated circuit density is to continue to increase into the next century, it is clear that fairly dramatic changes in the way transistors are fabricated and operated need to be made. This review has outlined strategies for fabricating transistors which operate by controlling the flow of single electrons. Research to date has shown that a single SET can function as an extremely sensitive electrometer and memory cell. If nanoscale electronics is to come to full fruition, however, three challenges must be met. First, if these devices are to operate near room temperature, large quantities of monodisperse nanoparticles less than 10 nm in diameter must be synthesized. Significant progress has been made toward this in the past few years. Second, methods must be developed for connecting the individual structures into patterns which function as logic circuits. Third, these circuits must in turn be arranged into larger 2D patterns. From both physical and economic perspectives, photo and electron beam lithographies are currently not suited to meet any of these challenges. Chemical self-assembly methods, however, are becoming quite adept at arranging large numbers of small structures into well-ordered macroscopic architectures. It is likely that these methods will have much to offer the chemist interested in designing more complex nanoparticle structures for use in advanced electronics.

6 Acknowledgements

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